FIG. 1

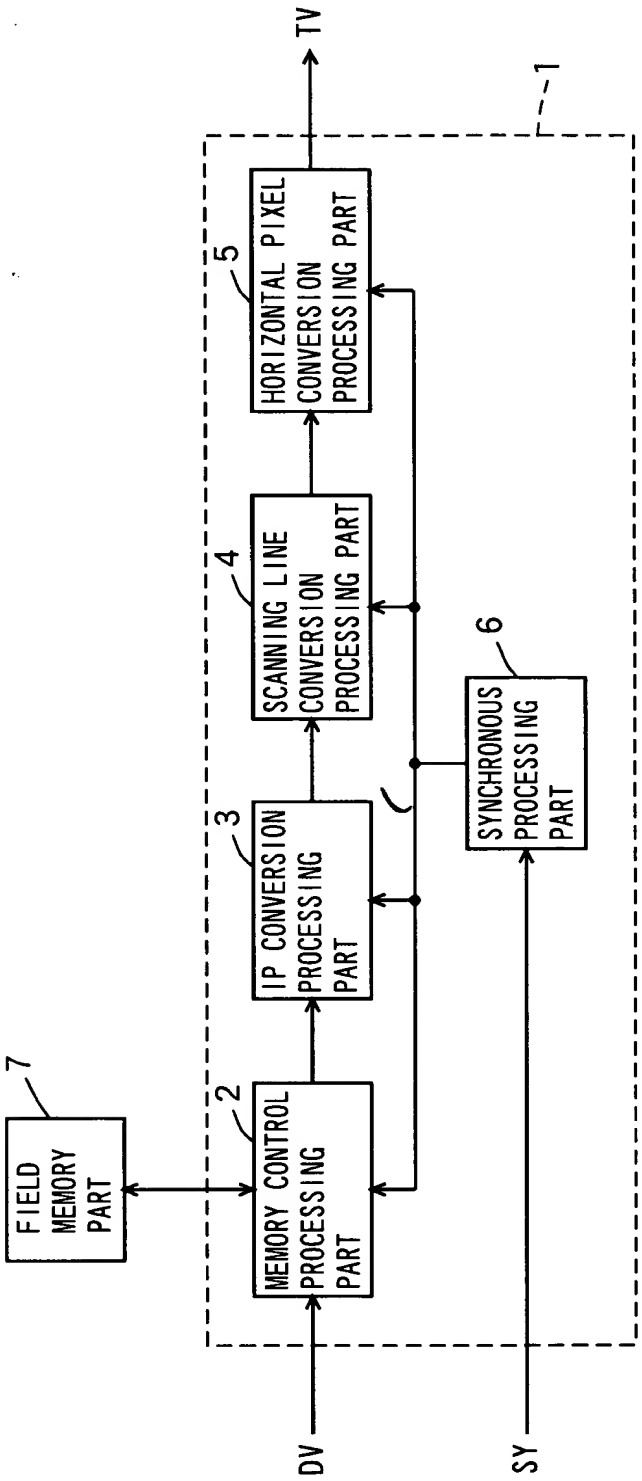

TV
1
HORIZONTAL PIXEL CONVERSION PROCESSING PART
5
SCANNING LINE CONVERSION PROCESSING PART
4
IP CONVERSION PROCESSING PART
3
SYNCHRONOUS PROCESSING PART
6
MEMORY CONTROL PROCESSING PART
2
FIELD MEMORY PART
7
DV
SY

FIG. 2

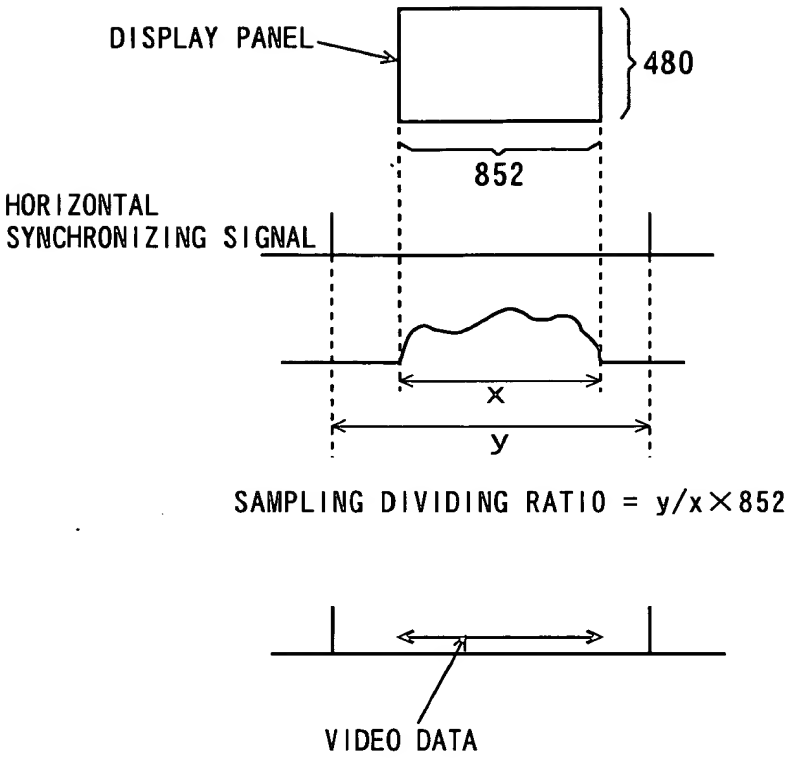

DISPLAY PANEL
480
852
HORIZONTAL
SYNCHRONIZING SIGNAL
x
y
SAMPLING DIVIDING RATIO = y/x×852
VIDEO DATA

FIG. 3

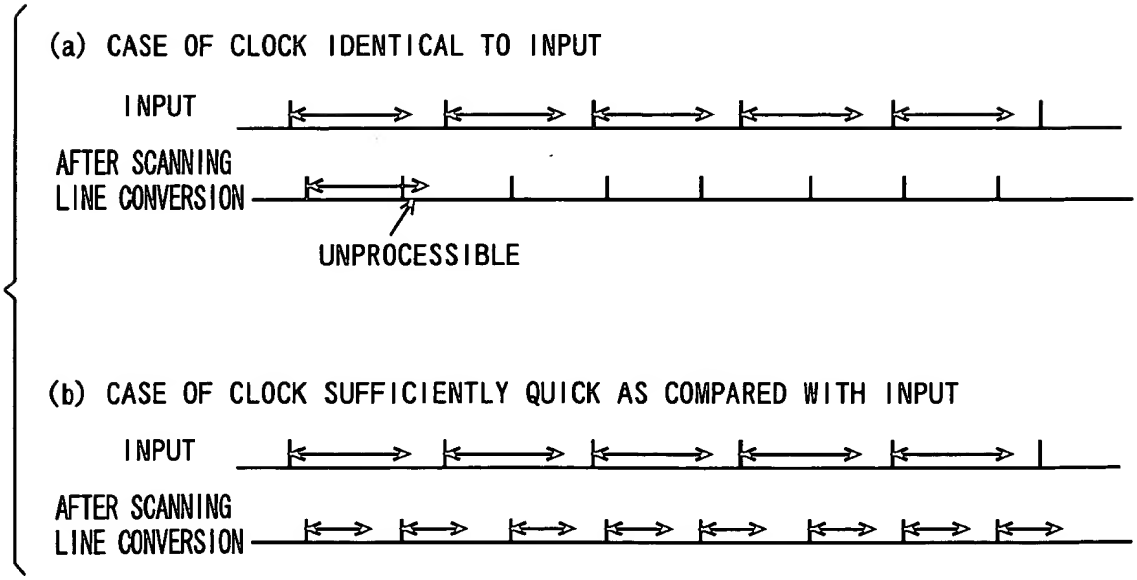

(a) CASE OF CLOCK IDENTICAL TO INPUT
INPUT
AFTER SCANNING
LINE CONVERSION
UNPROCESSIBLE
(b) CASE OF CLOCK SUFFICIENTLY QUICK AS COMPARED WITH INPUT
INPUT
AFTER SCANNING
LINE CONVERSION

FIG. 4

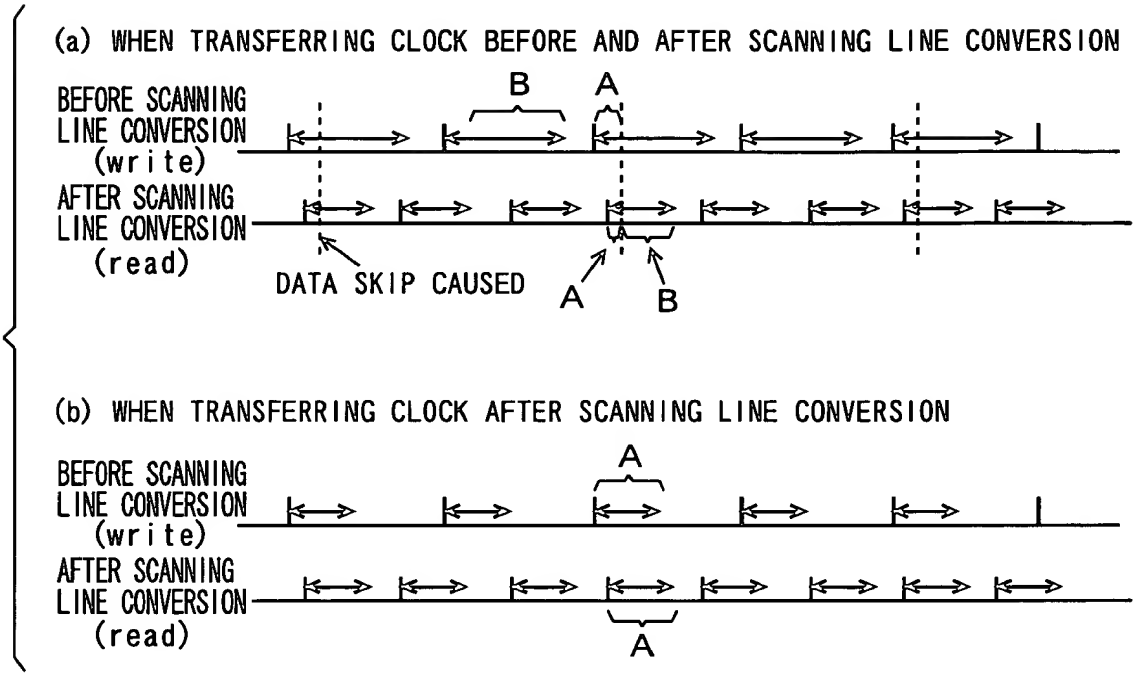
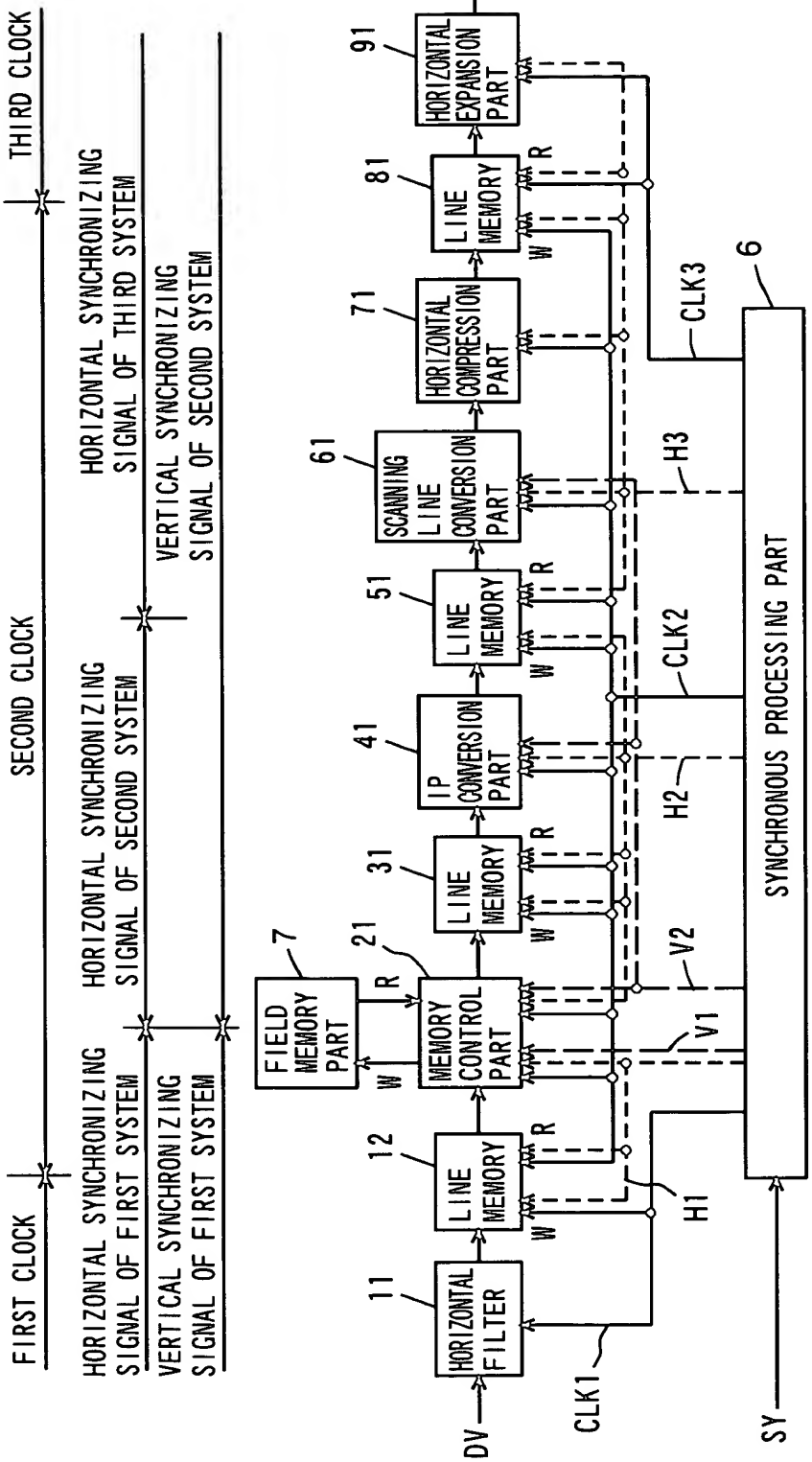

(a) WHEN TRANSFERRING CLOCK BEFORE AND AFTER SCANNING LINE CONVERSION
BEFORE SCANNING LINE CONVERSION (write)
AFTER SCANNING LINE CONVERSION (read)
B
A
DATA SKIP CAUSED
A
B
(b) WHEN TRANSFERRING CLOCK AFTER SCANNING LINE CONVERSION
BEFORE SCANNING LINE CONVERSION (write)
AFTER SCANNING LINE CONVERSION (read)
A
A

FIG. 5


FIRST CLOCK
SECOND CLOCK
THIRD CLOCK
HORIZONTAL SYNCHRONIZING SIGNAL OF FIRST SYSTEM
VERTICAL SYNCHRONIZING SIGNAL OF FIRST SYSTEM
HORIZONTAL SYNCHRONIZING SIGNAL OF SECOND SYSTEM
VERTICAL SYNCHRONIZING SIGNAL OF SECOND SYSTEM
HORIZONTAL SYNCHRONIZING SIGNAL OF THIRD SYSTEM
DV
CLK1
SY
TV
HORIZONTAL FILTER
LINE MEMORY
MEMORY CONTROL PART
FIELD MEMORY PART
IP CONVERSION PART
SCANNING LINE CONVERSION PART
HORIZONTAL COMPRESSION PART
HORIZONTAL EXPANSION PART
SYNCHRONOUS PROCESSING PART
11
12
21
31
41
51
61
71
81
91
7
6
W
R
H1
H2
H3
V1
V2
CLK2
CLK3

09/889585

FIG. 6

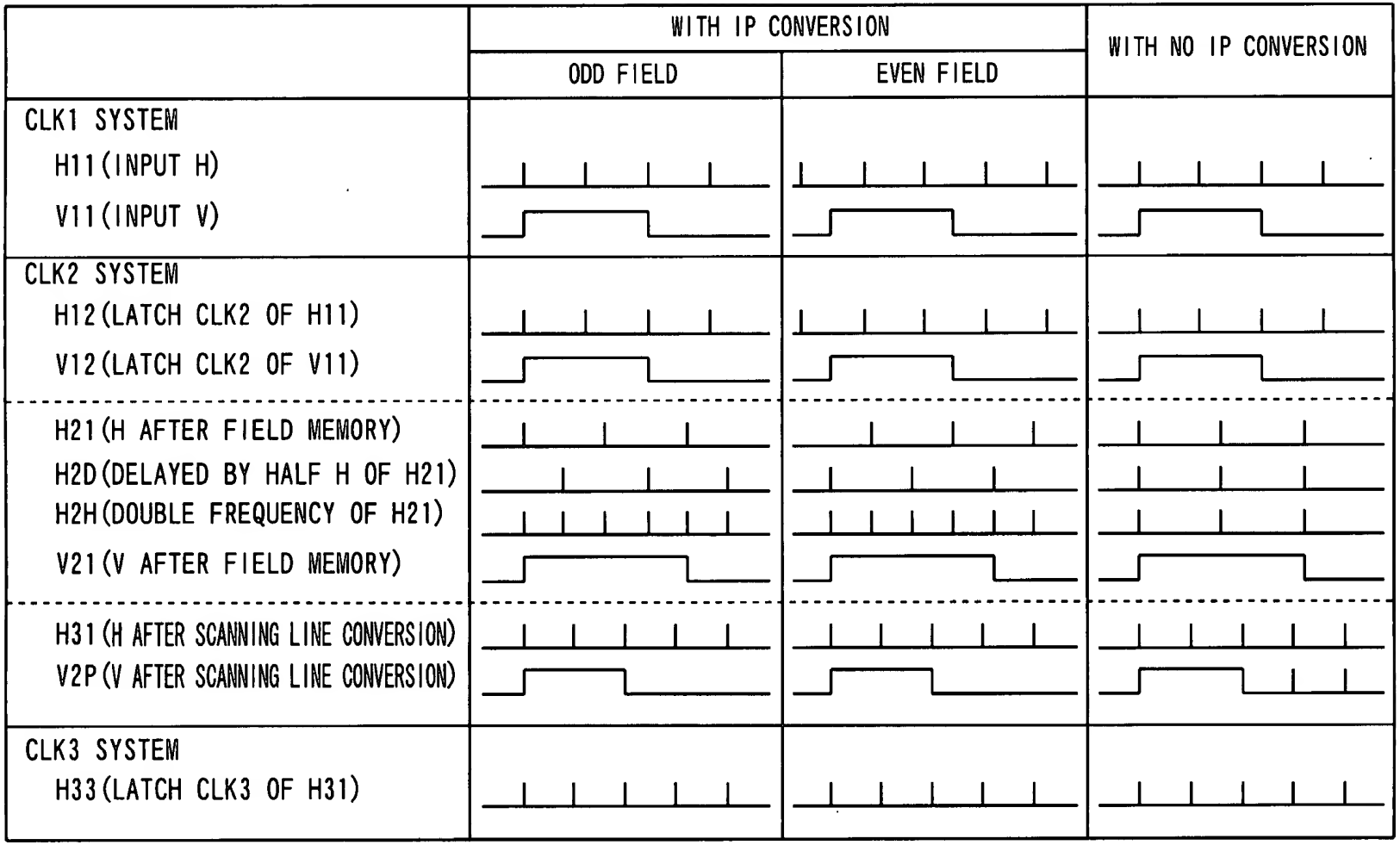


FIG. 7

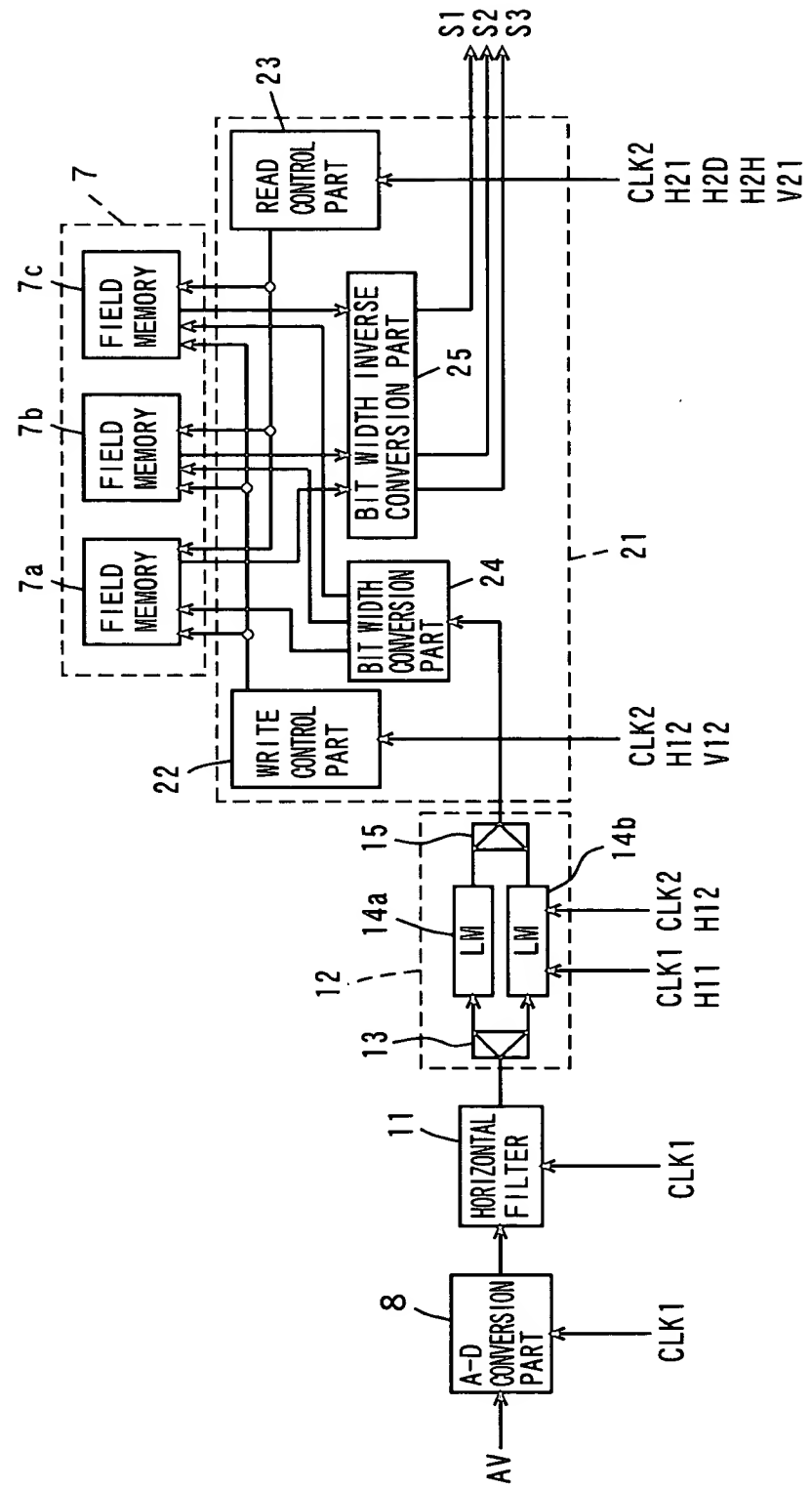

AV
A-D CONVERSION PART
8
CLK1
HORIZONTAL FILTER
11
CLK1
13
12
14a
LM
LM
15
14b
CLK1 CLK2
H11 H12
WRITE CONTROL PART
22
CLK2
H12
V12
21
BIT WIDTH CONVERSION PART
24
BIT WIDTH INVERSE CONVERSION PART
25
FIELD MEMORY
7a
FIELD MEMORY
7b
FIELD MEMORY
7c
7
READ CONTROL PART
23
CLK2
H21
H2D
H2H
V21
S1
S2
S3

FIG. 8

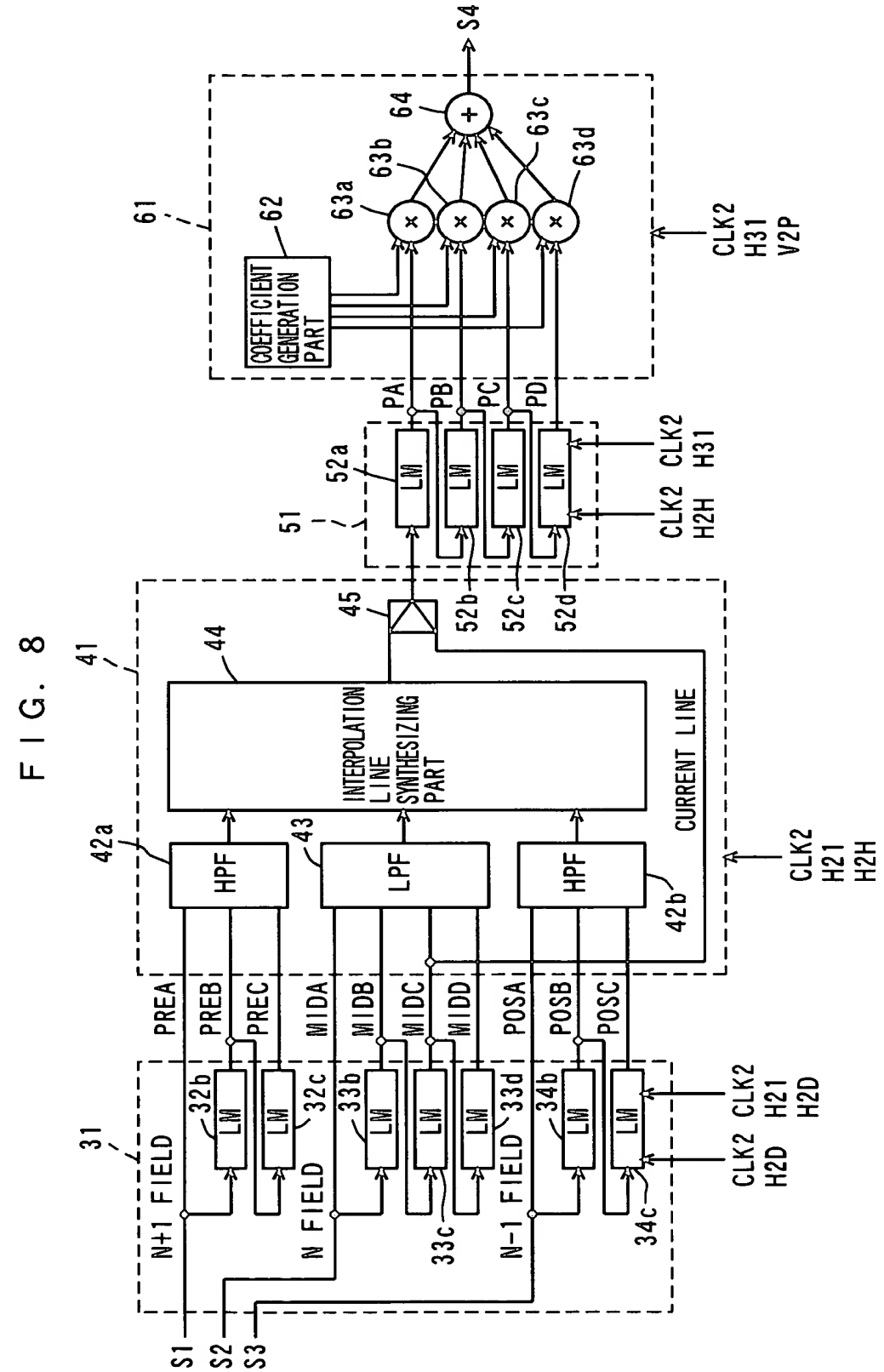

S1
S2
S3
S4
N+1 FIELD
N FIELD
N-1 FIELD
PREA
PREB
PREC
MIDA
MIDB
MIDC
MIDD
POSA
POSB
POSC
HPF
LPF
HPF
INTERPOLATION LINE SYNTHESIZING PART
CURRENT LINE
LM
COEFFICIENT GENERATION PART
PA
PB
PC
PD
CLK2
H21
H2H
H2D
H31
V2P
31
32b
32c
33b
33c
33d
34b
34c
41
42a
42b
43
44
45
51
52a
52b
52c
52d
61
62
63a
63b
63c
63d
64

FIG. 9

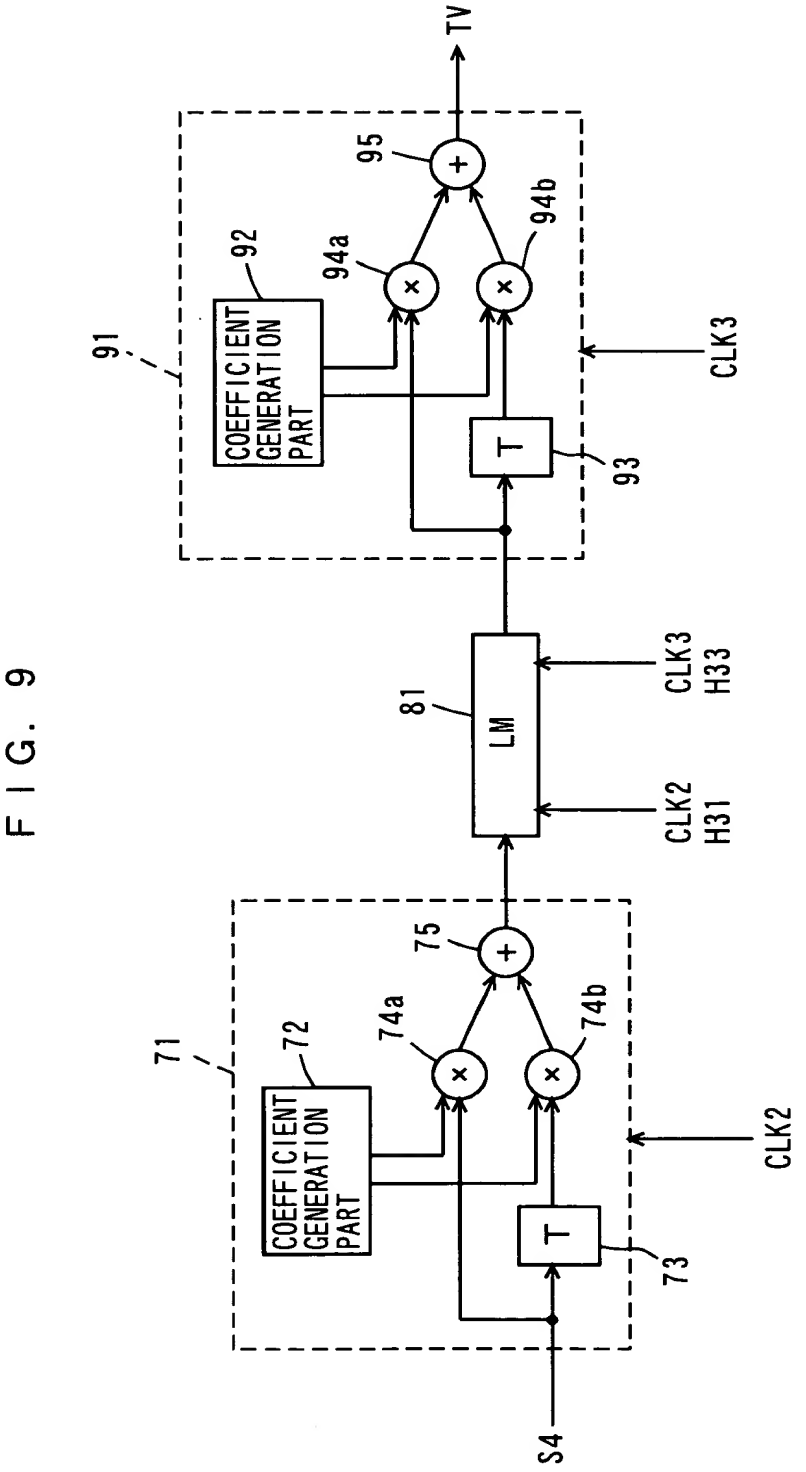

TV
95
94a
94b
92
91
COEFFICIENT GENERATION PART
T
93
CLK3
81
LM
CLK3
H33
CLK2
H31
75
74a
74b
72
71
COEFFICIENT GENERATION PART
T
73
CLK2
S4

FIG. 10

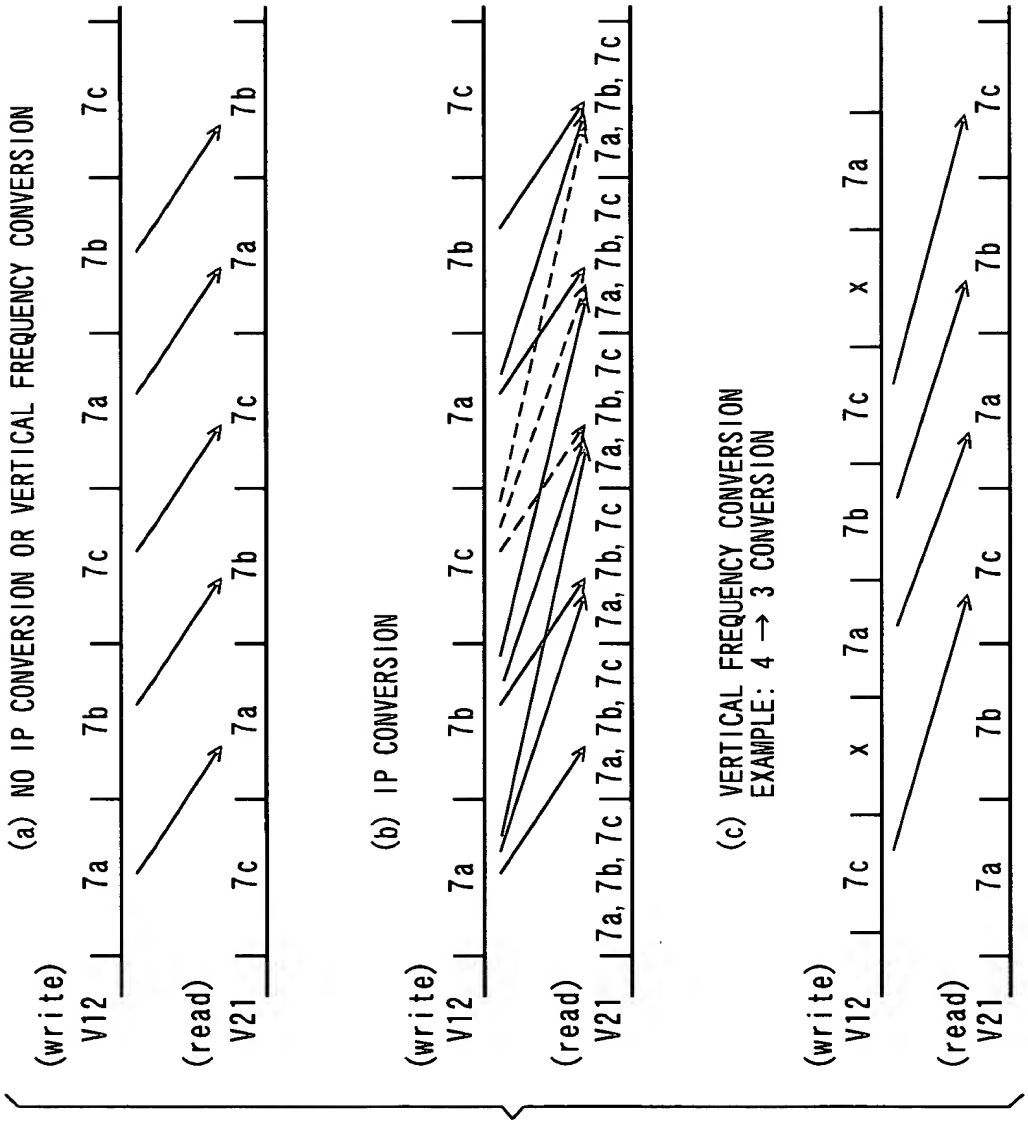

(a) NO IP CONVERSION OR VERTICAL FREQUENCY CONVERSION
(write)
V12
7a
7b
7c
7a
7b
7c
(read)
V21
7c
7a
7b
7c
7a
7b
(b) IP CONVERSION
(write)
V12
7a
7b
7c
7a
7b
7c
(read)
V21
7a, 7b, 7c
7a, 7b, 7c
7a, 7b, 7c
7a, 7b, 7c
7a, 7b, 7c
7a, 7b, 7c
(c) VERTICAL FREQUENCY CONVERSION
EXAMPLE: 4 → 3 CONVERSION
(write)
V12
7c
x
7a
7b
7c
x
7a
(read)
V21
7a
7b
7c
7a
7b
7c

FIG. 11

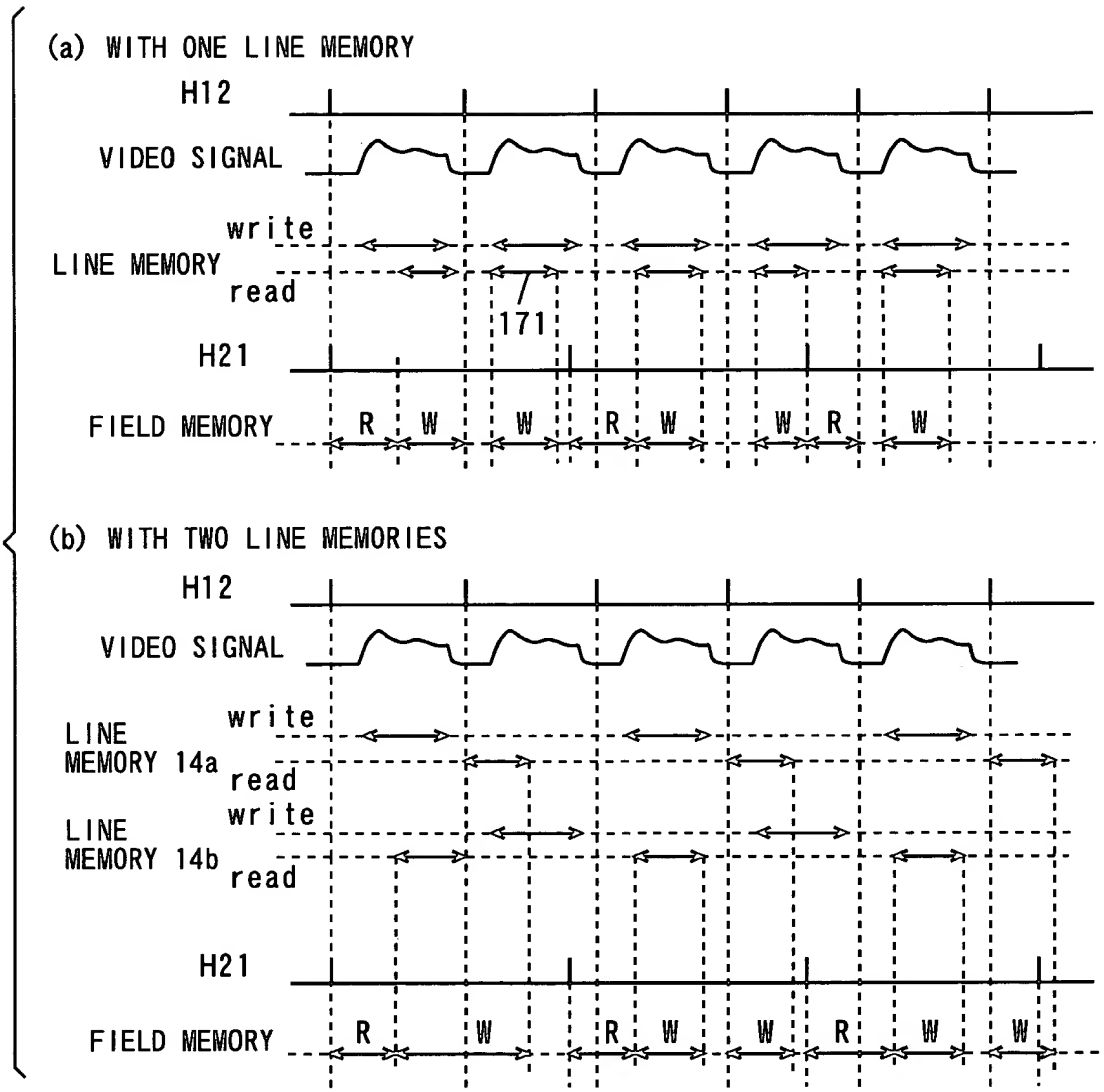

(a) WITH ONE LINE MEMORY
H12
VIDEO SIGNAL
write
LINE MEMORY
read
171
H21
FIELD MEMORY
R
W
W
R
W
W
R
W
(b) WITH TWO LINE MEMORIES
H12
VIDEO SIGNAL
write
LINE MEMORY 14a
read
write
LINE MEMORY 14b
read
H21
FIELD MEMORY
R
W
R
W
W
R
W
W

FIG. 12

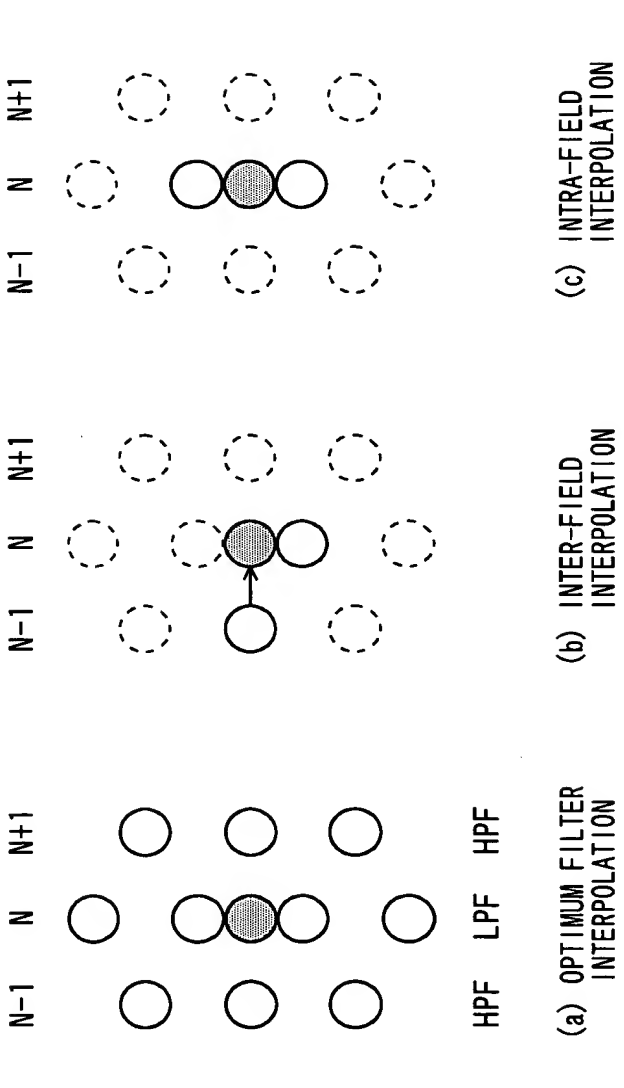
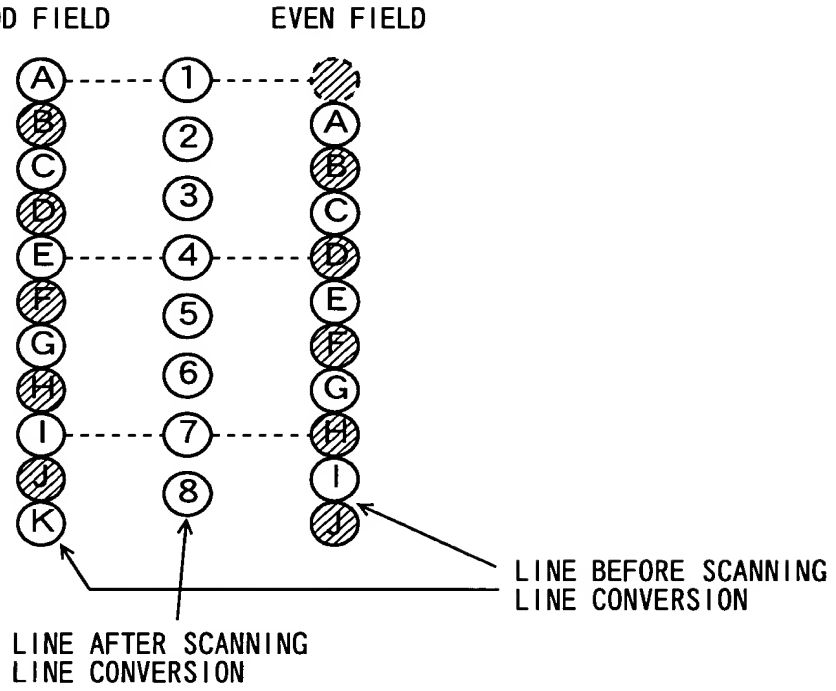

N-1
N
N+1
HPF
LPF
HPF
(a) OPTIMUM FILTER INTERPOLATION
N-1
N
N+1
(b) INTER-FIELD INTERPOLATION
N-1
N
N+1
(c) INTRA-FIELD INTERPOLATION

FIG. 13



JP2000-244905

FIG. 14

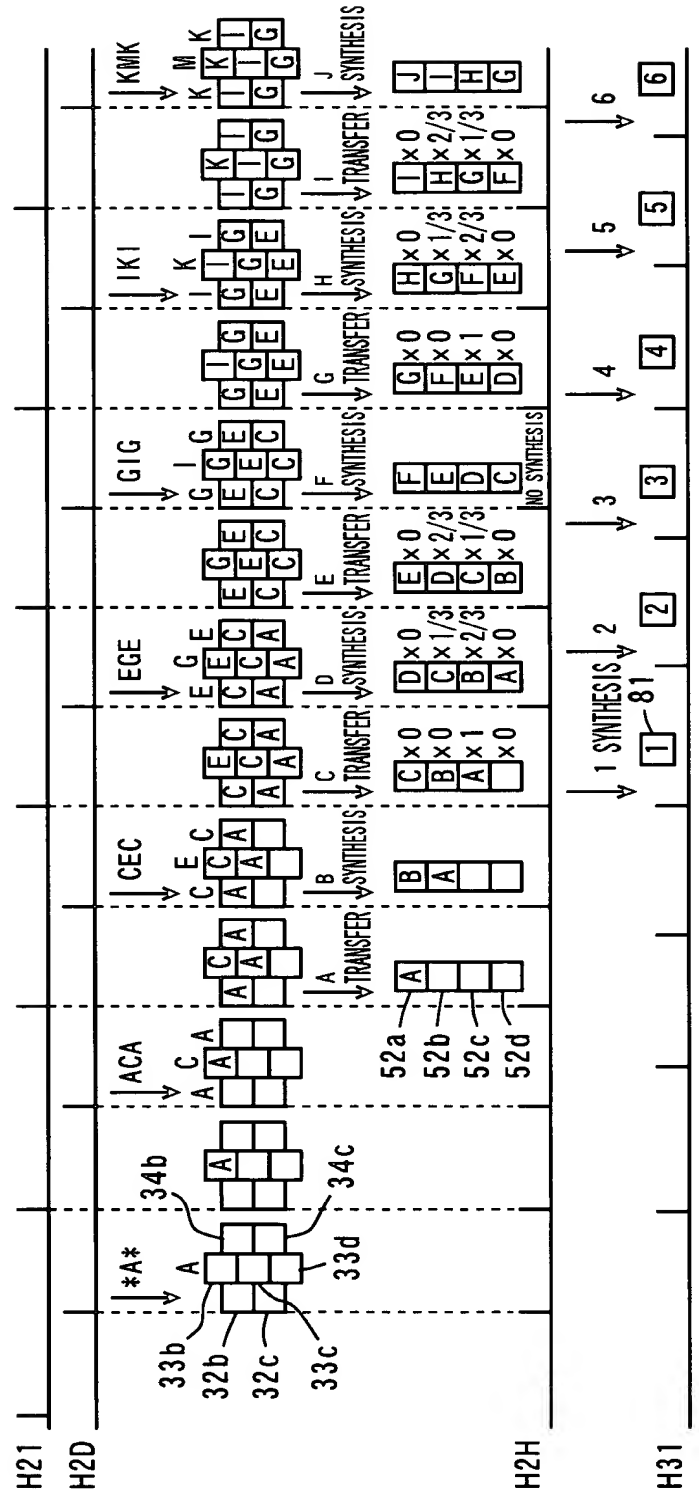

H21
H2D
H2H
H31
A
ACA
CEC
EGE
G1G
IK1
KMK
TRANSFER
SYNTHESIS
NO SYNTHESIS
1 SYNTHESIS
81
33b
32b
32c
33c
33d
34b
34c
52a
52b
52c
52d

FIG. 15

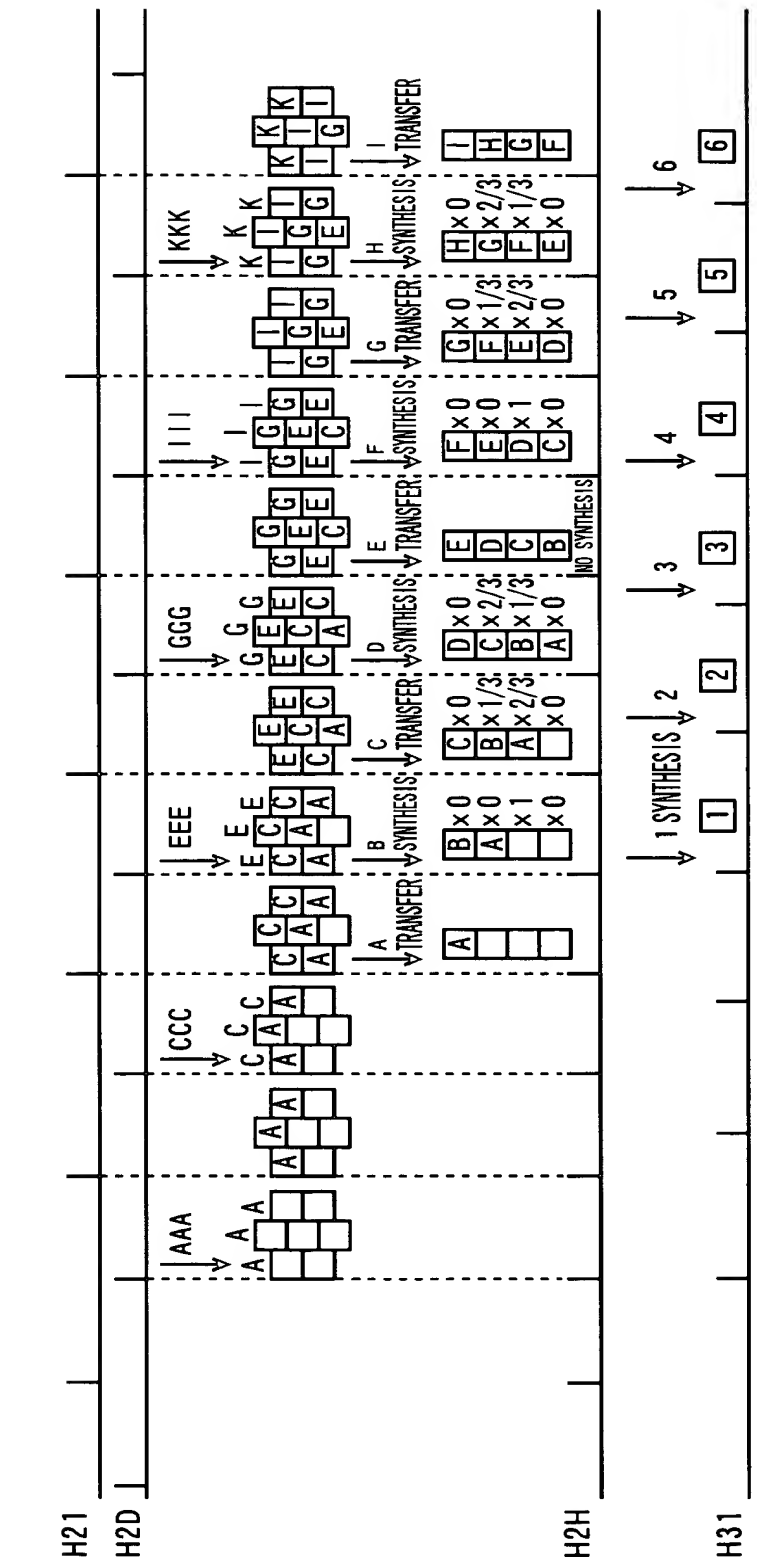

H21
H2D
H2H
H31
AAA
CCC
EEE
GGG
III
KKK
TRANSFER
SYNTHESIS
NO SYNTHESIS
1 SYNTHESIS
A
B
C
D
E
F
G
H
I
1
2
3
4
5
6

FIG. 16

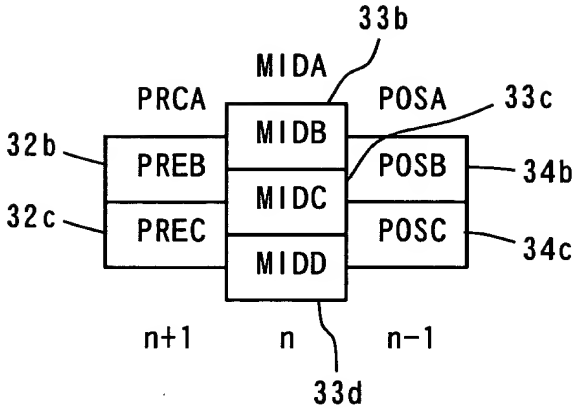

33b
MIDA
PRCA
POSA
33c
32b
MIDB
PREB
POSB
34b
32c
MIDC
PREC
POSC
34c
MIDD
n+1
n
n-1
33d

FIG. 17

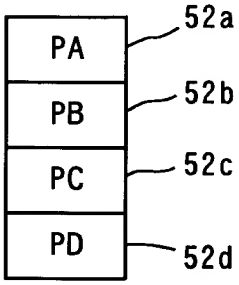

52a
PA
52b
PB
52c
PC
52d
PD

FIG. 18

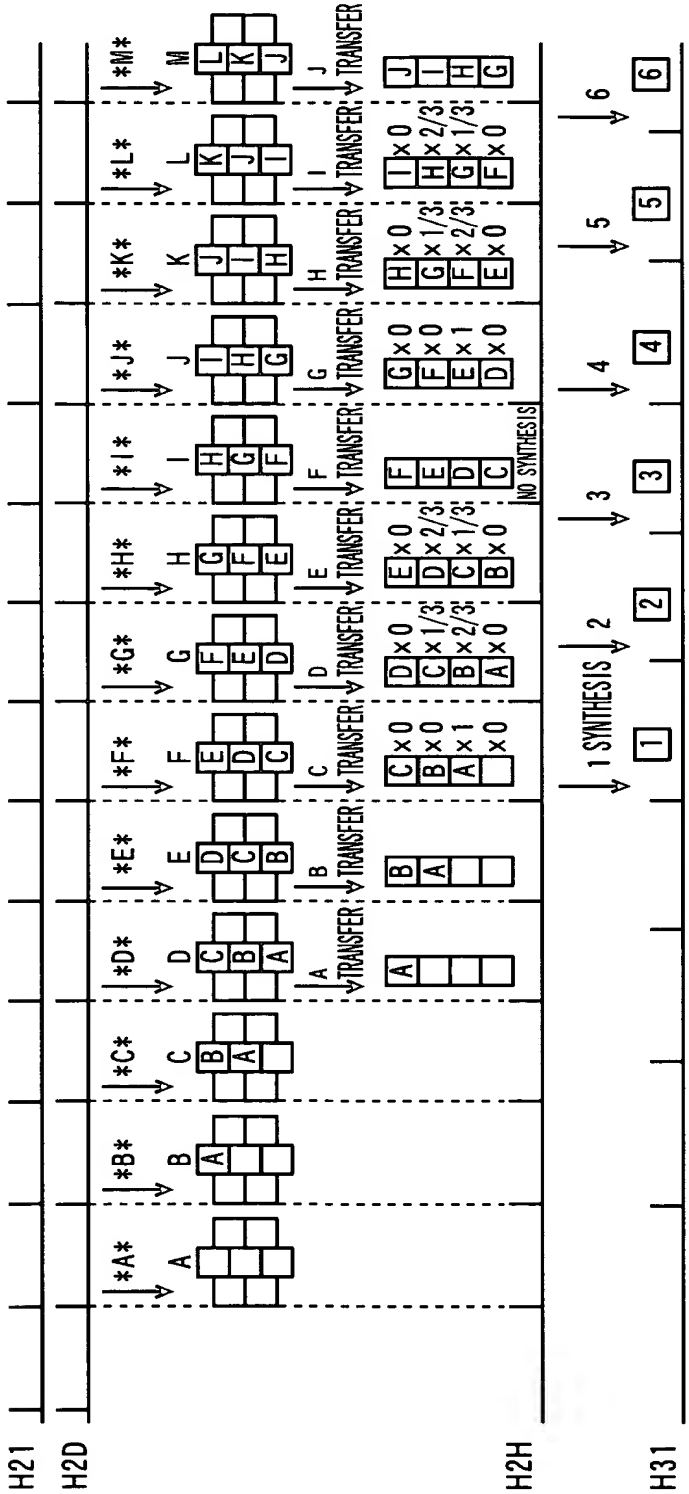
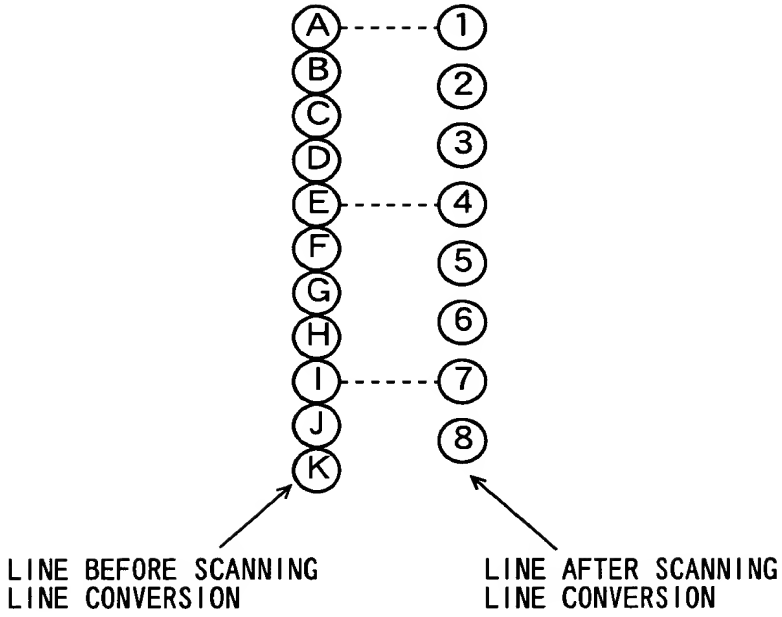

H21
H2D
H2H
H31
A
B
C
D
E
F
G
H
I
J
K
L
M
TRANSFER
NO SYNTHESIS
1 SYNTHESIS
2
3
4
5
6

FIG. 19



09889585 - 042404

FIG. 20

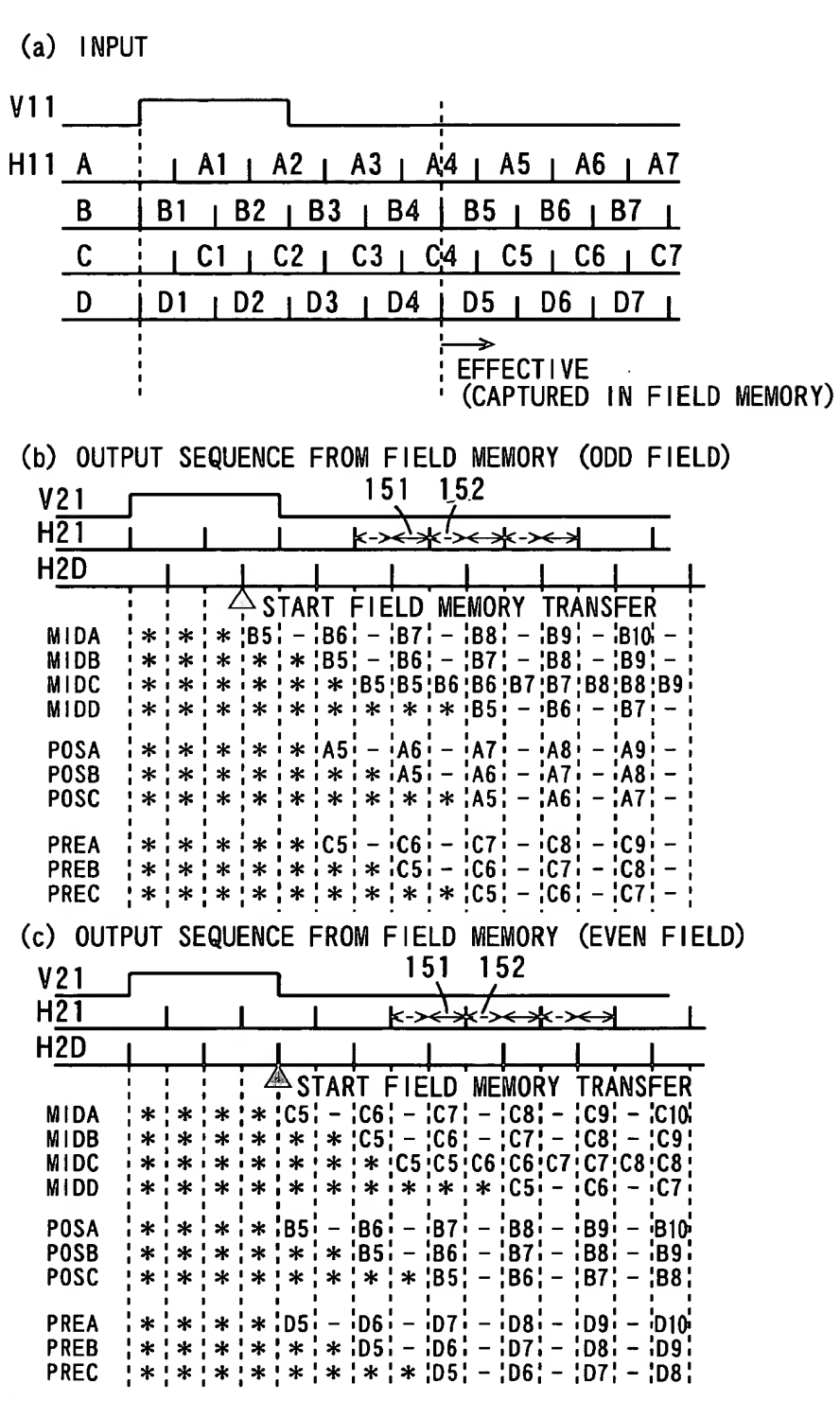

(a) INPUT
V11
H11
A A1 A2 A3 A4 A5 A6 A7
B B1 B2 B3 B4 B5 B6 B7
C C1 C2 C3 C4 C5 C6 C7
D D1 D2 D3 D4 D5 D6 D7
EFFECTIVE
(CAPTURED IN FIELD MEMORY)
(b) OUTPUT SEQUENCE FROM FIELD MEMORY (ODD FIELD)
V21
H21
H2D
151 152
START FIELD MEMORY TRANSFER
MIDA * * * B5 - B6 - B7 - B8 - B9 - B10 -
MIDB * * * * * B5 - B6 - B7 - B8 - B9 -
MIDC * * * * * * B5 B5 B6 B6 B7 B7 B8 B8 B9
MIDD * * * * * * * * * B5 - B6 - B7 -
POSA * * * * * A5 - A6 - A7 - A8 - A9 -
POSB * * * * * * * A5 - A6 - A7 - A8 -
POSC * * * * * * * * * A5 - A6 - A7 -
PREA * * * * * C5 - C6 - C7 - C8 - C9 -
PREB * * * * * * * C5 - C6 - C7 - C8 -
PREC * * * * * * * * * C5 - C6 - C7 -
(c) OUTPUT SEQUENCE FROM FIELD MEMORY (EVEN FIELD)
V21
H21
H2D
151 152
START FIELD MEMORY TRANSFER
MIDA * * * * C5 - C6 - C7 - C8 - C9 - C10
MIDB * * * * * * C5 - C6 - C7 - C8 - C9
MIDC * * * * * * * C5 C5 C6 C6 C7 C7 C8 C8
MIDD * * * * * * * * * * C5 - C6 - C7
POSA * * * * B5 - B6 - B7 - B8 - B9 - B10
POSB * * * * * * B5 - B6 - B7 - B8 - B9
POSC * * * * * * * * B5 - B6 - B7 - B8
PREA * * * * D5 - D6 - D7 - D8 - D9 - D10
PREB * * * * * * D5 - D6 - D7 - D8 - D9
PREC * * * * * * * * D5 - D6 - D7 - D8

FIG. 21

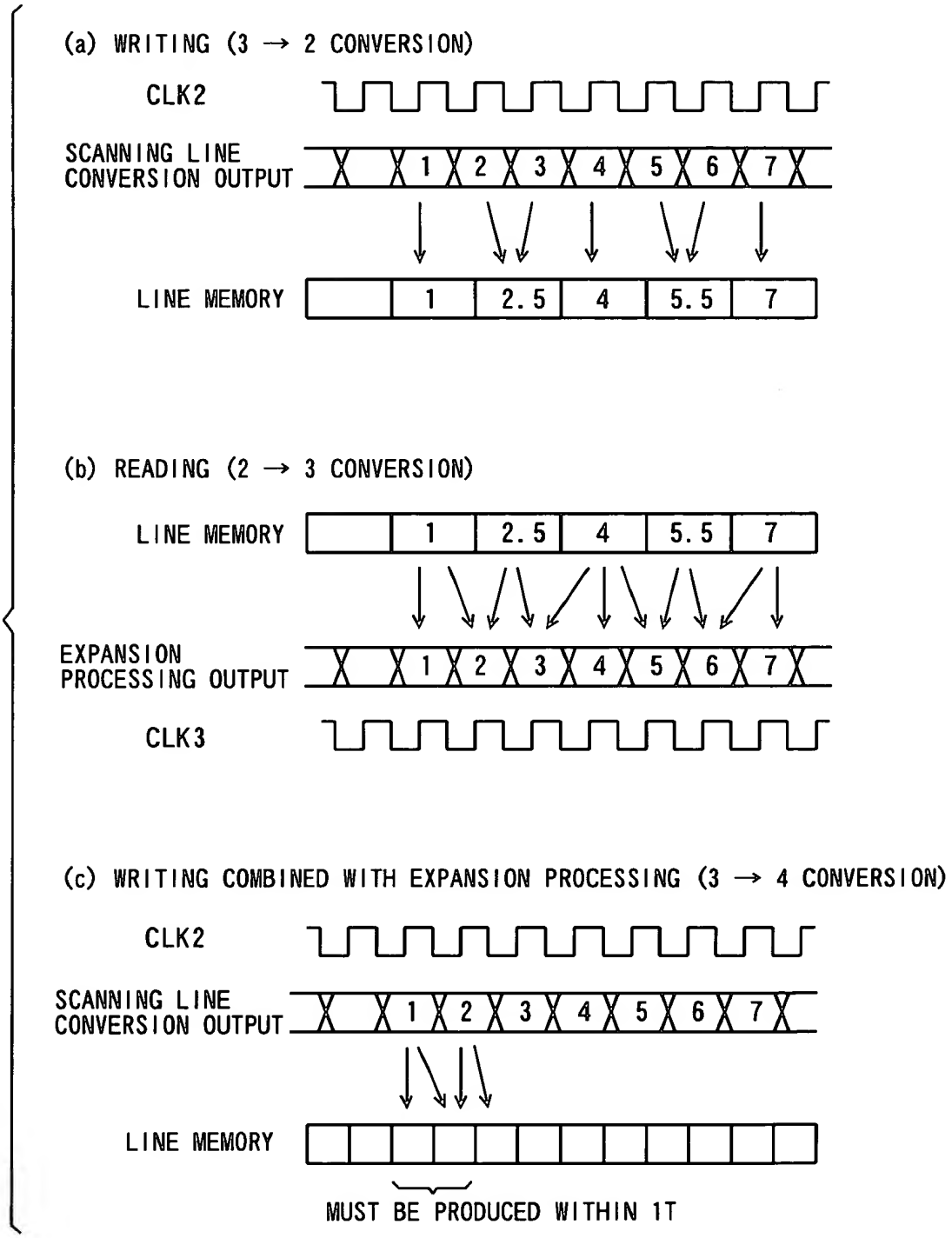

(a) WRITING (3 → 2 CONVERSION)
CLK2
SCANNING LINE CONVERSION OUTPUT
1 2 3 4 5 6 7
LINE MEMORY
1 2.5 4 5.5 7
(b) READING (2 → 3 CONVERSION)
LINE MEMORY
1 2.5 4 5.5 7
EXPANSION PROCESSING OUTPUT
1 2 3 4 5 6 7
CLK3
(c) WRITING COMBINED WITH EXPANSION PROCESSING (3 → 4 CONVERSION)
CLK2
SCANNING LINE CONVERSION OUTPUT
1 2 3 4 5 6 7
LINE MEMORY
MUST BE PRODUCED WITHIN 1T

FIG. 22

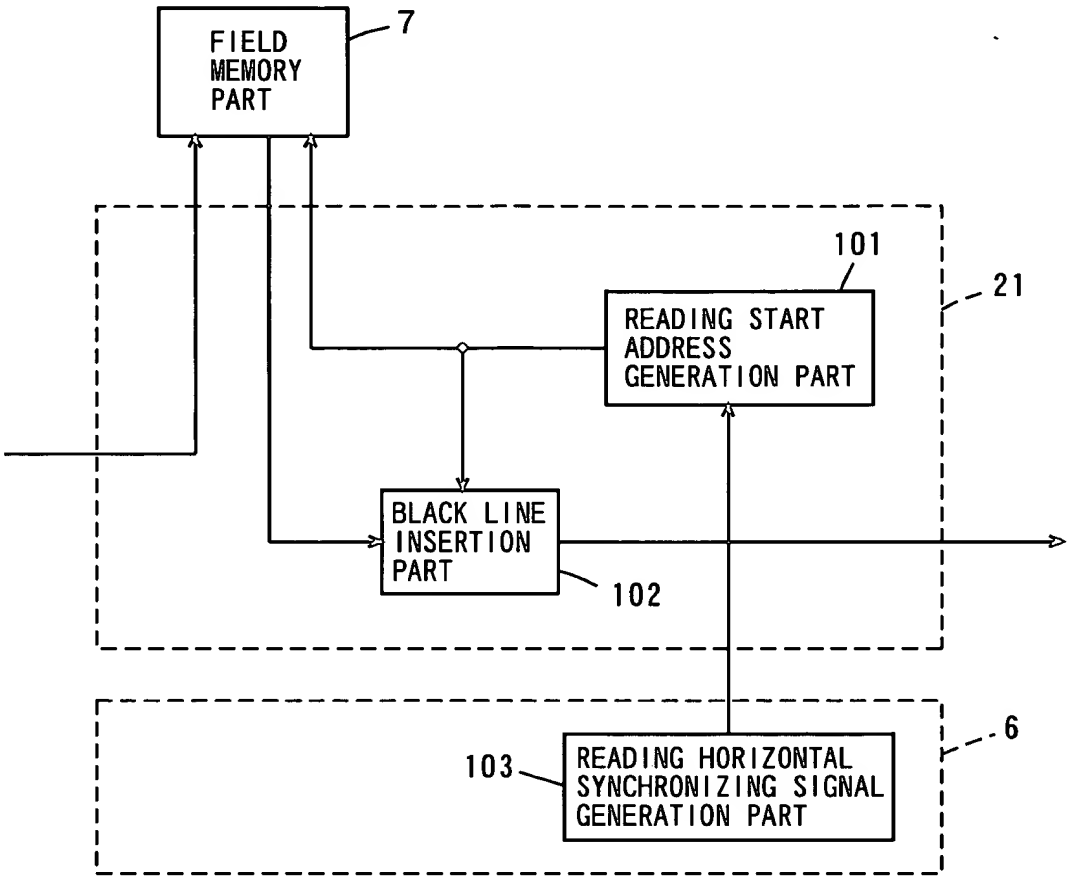

FIELD MEMORY PART
7
101
21
READING START ADDRESS GENERATION PART
BLACK LINE INSERTION PART
102
6
103
READING HORIZONTAL SYNCHRONIZING SIGNAL GENERATION PART

FIG. 23

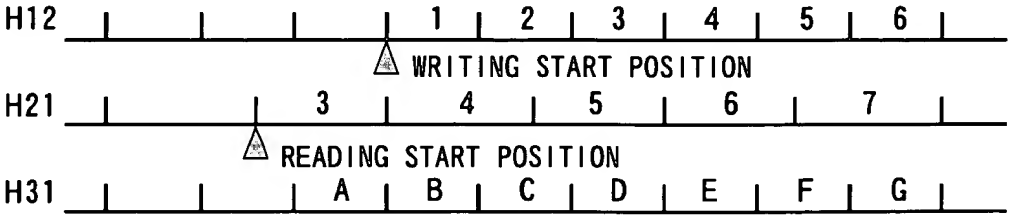

H12
1
2
3
4
5
6
WRITING START POSITION
H21
3
4
5
6
7
READING START POSITION
H31
A
B
C
D
E
F
G

FIG. 24

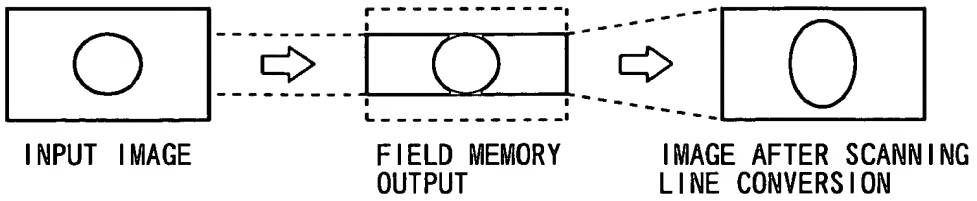


FIG. 25

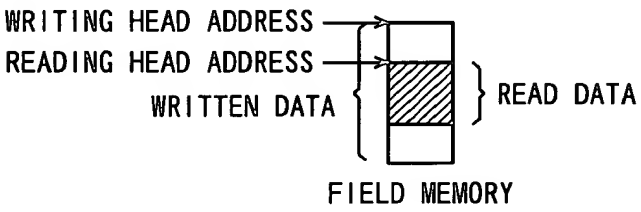


FIG. 26

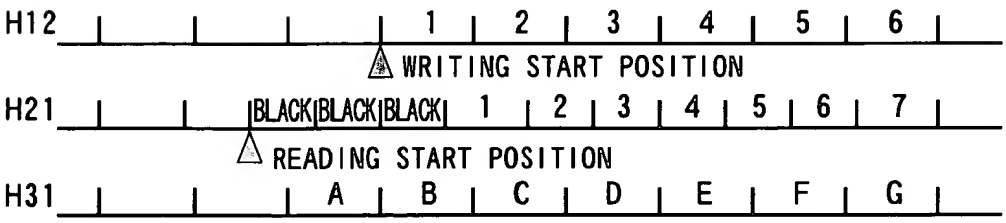


FIG. 27

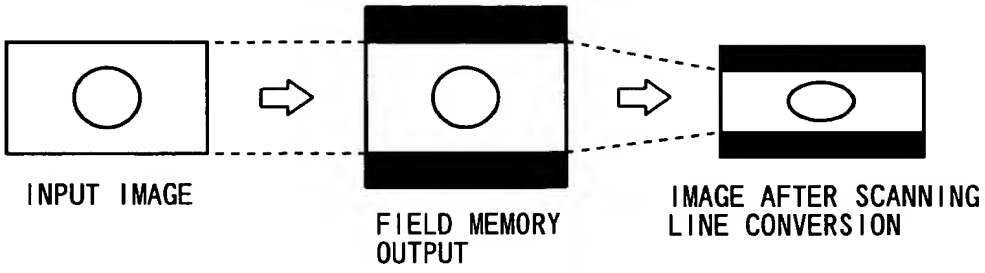

INPUT IMAGE
FIELD MEMORY OUTPUT
IMAGE AFTER SCANNING LINE CONVERSION

FIG. 28

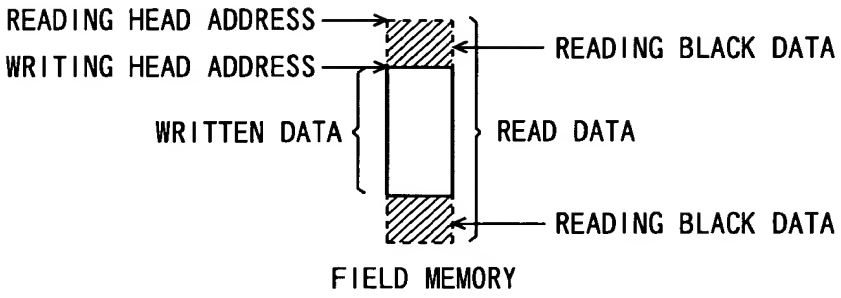

READING HEAD ADDRESS
WRITING HEAD ADDRESS
WRITTEN DATA
READ DATA
READING BLACK DATA
READING BLACK DATA
FIELD MEMORY

FIG. 29

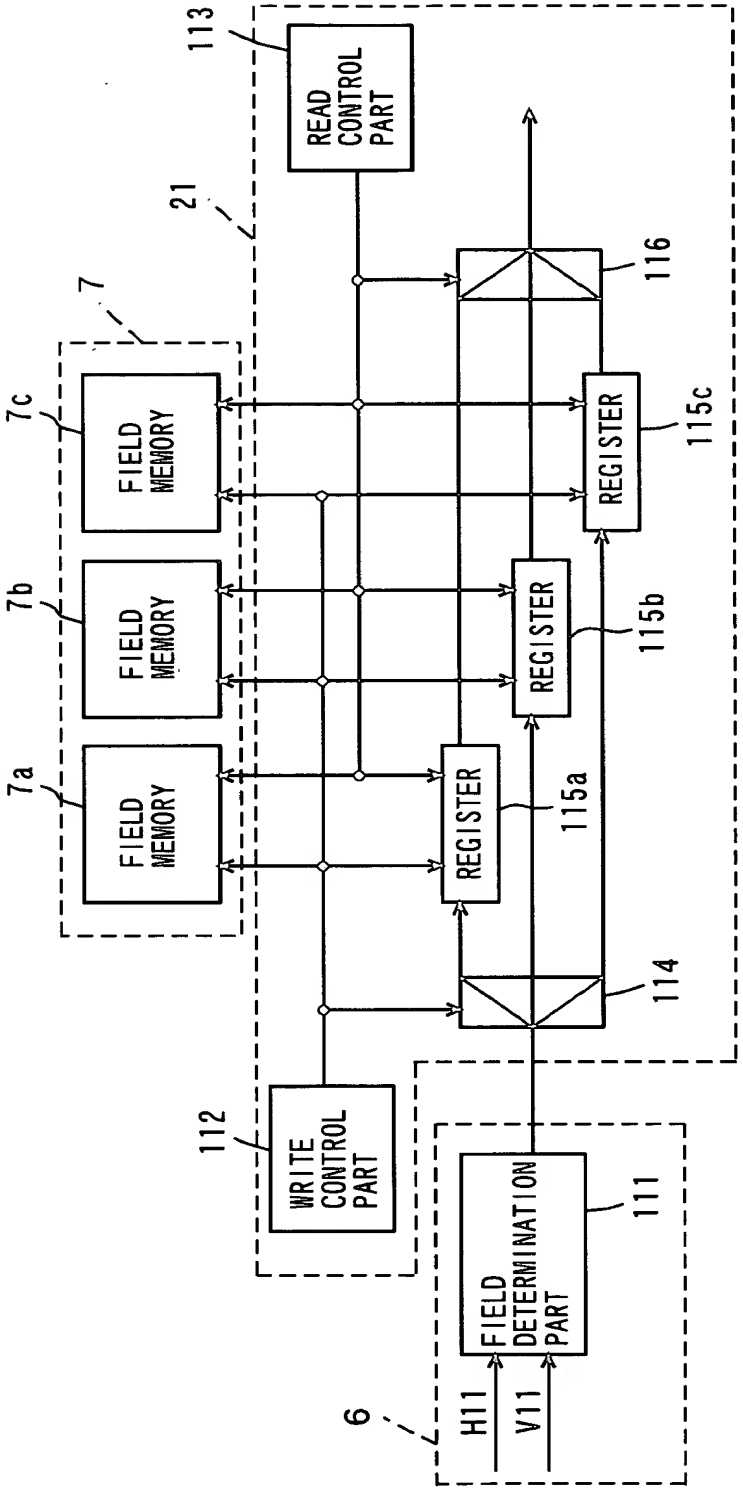

READ CONTROL PART
113
21
7
7c
FIELD MEMORY
7b
FIELD MEMORY
7a
FIELD MEMORY
116
REGISTER
115c
REGISTER
115b
REGISTER
115a
114
WRITE CONTROL PART
112
FIELD DETERMINATION PART
111
H11
V11
6

FIG. 30

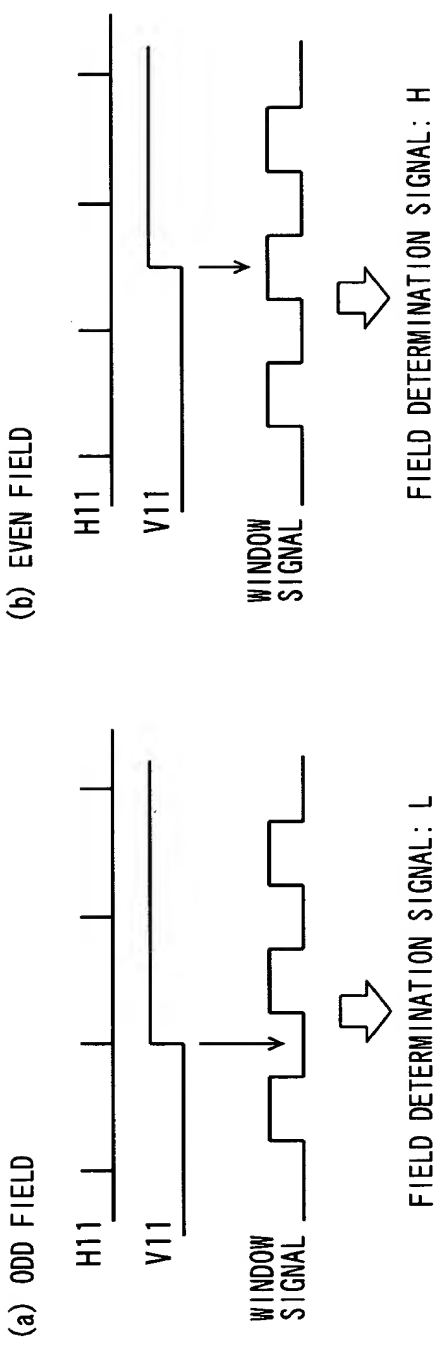

(a) ODD FIELD
H11
V11
WINDOW SIGNAL
FIELD DETERMINATION SIGNAL: L
(b) EVEN FIELD
H11
V11
WINDOW SIGNAL
FIELD DETERMINATION SIGNAL: H

FIG. 31

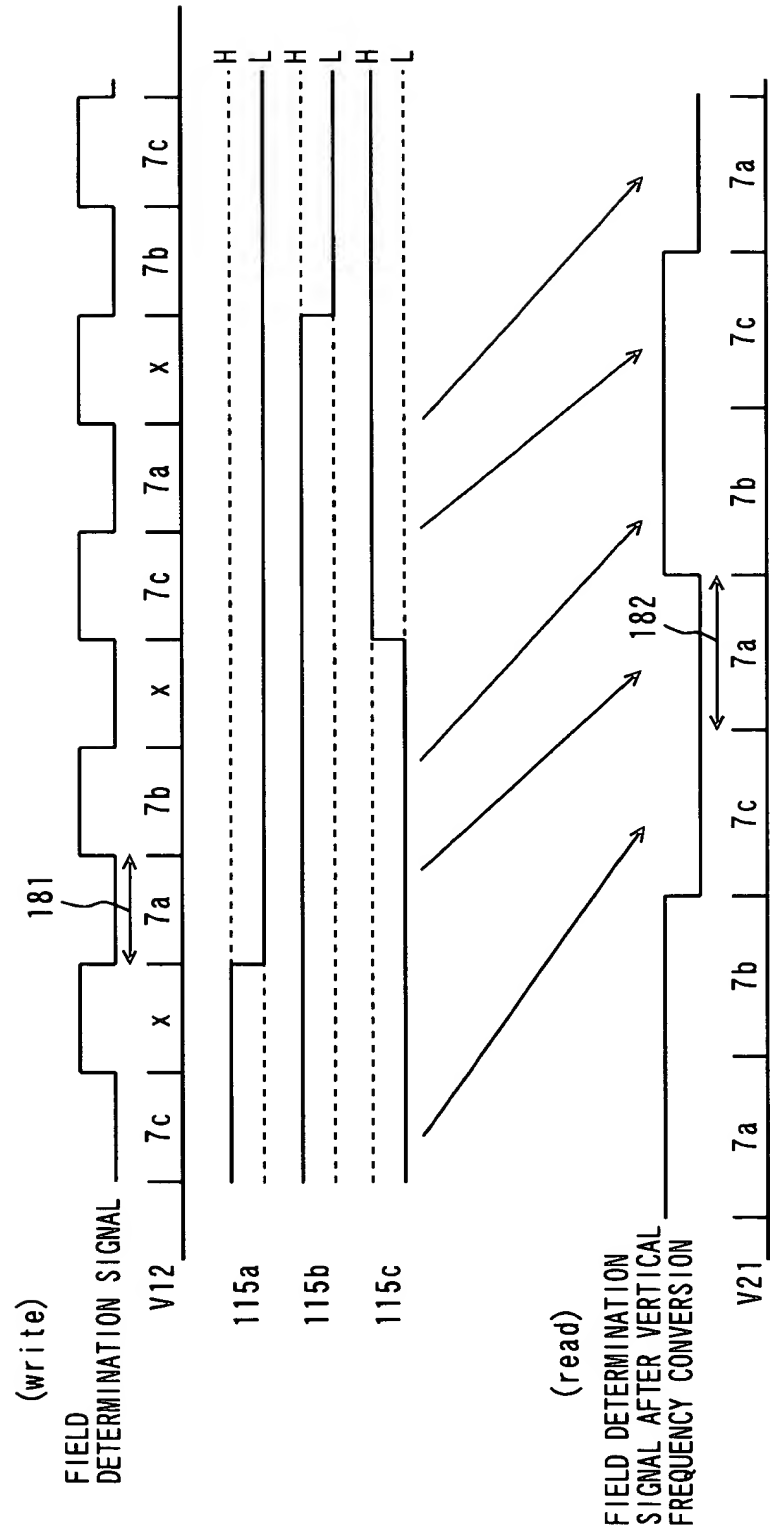

(write)
FIELD DETERMINATION SIGNAL
V12
181
7c
x
7a
7b
x
7c
7a
x
7b
7c
115a
115b
115c
H
L
(read)
FIELD DETERMINATION SIGNAL AFTER VERTICAL FREQUENCY CONVERSION
V21
182
7a
7b
7c
7a
7b
7c
7a

FIG. 32

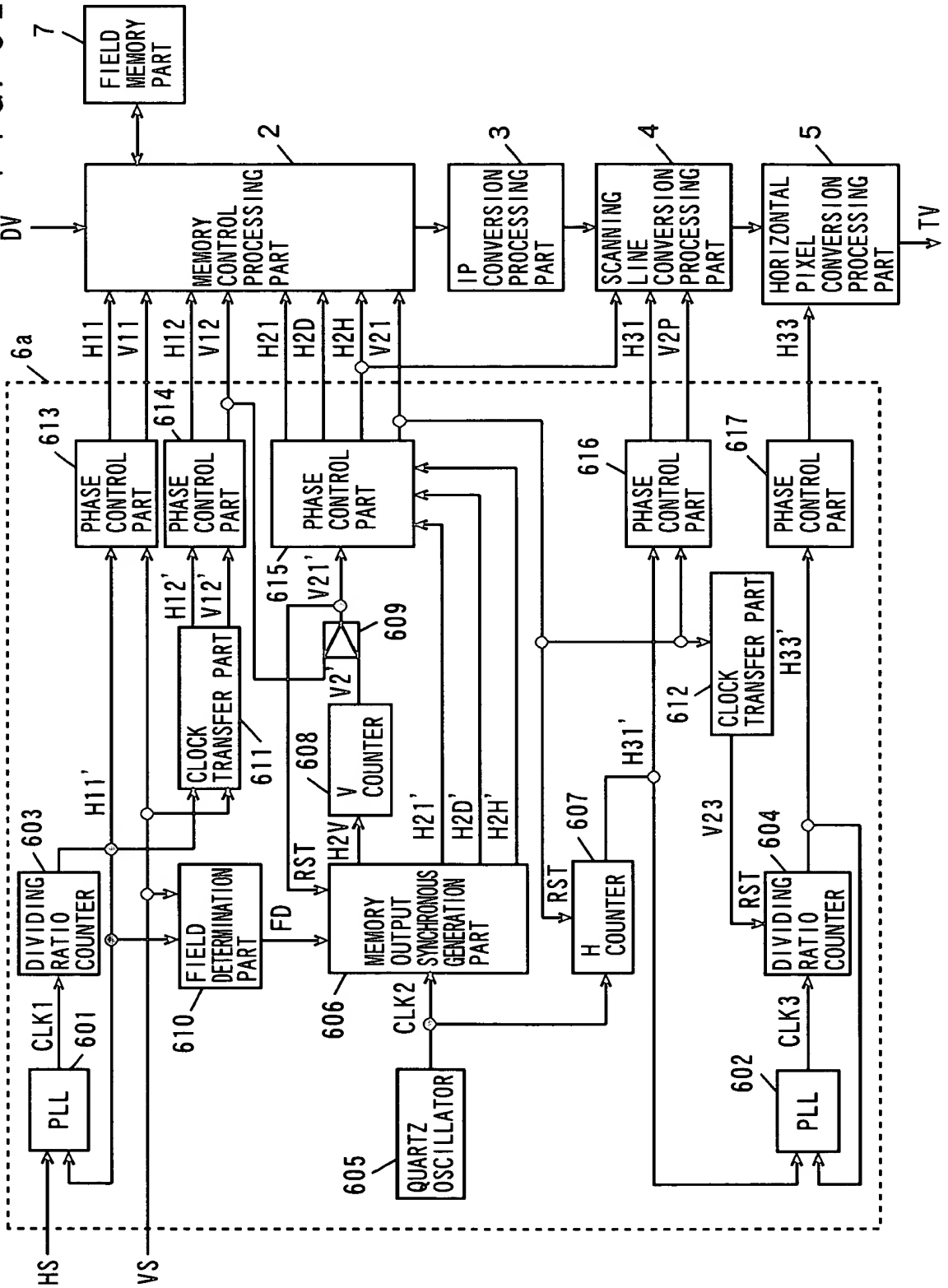

7
FIELD MEMORY PART
DV
2
MEMORY CONTROL PROCESSING PART
3
IP CONVERSION PROCESSING PART
4
SCANNING LINE CONVERSION PROCESSING PART
5
HORIZONTAL PIXEL CONVERSION PROCESSING PART
TV
6a
H11
V11
H12
V12
H21
H2D
H2H
V21
H31
V2P
H33
613
PHASE CONTROL PART
614
PHASE CONTROL PART
PHASE CONTROL PART
616
PHASE CONTROL PART
617
PHASE CONTROL PART
H12'
V12'
615
V21'
609
V2'
CLOCK TRANSFER PART
611
608
V COUNTER
612
CLOCK TRANSFER PART
H33'
H11'
603
DIVIDING RATIO COUNTER
FIELD DETERMINATION PART
FD
RST
H2V
H21'
H2D'
H2H'
MEMORY OUTPUT SYNCHRONOUS GENERATION PART
607
H COUNTER
H31'
V23
604
DIVIDING RATIO COUNTER
CLK1
601
PLL
610
606
CLK2
QUARTZ OSCILLATOR
605
602
CLK3
PLL
HS
VS

FIG. 33

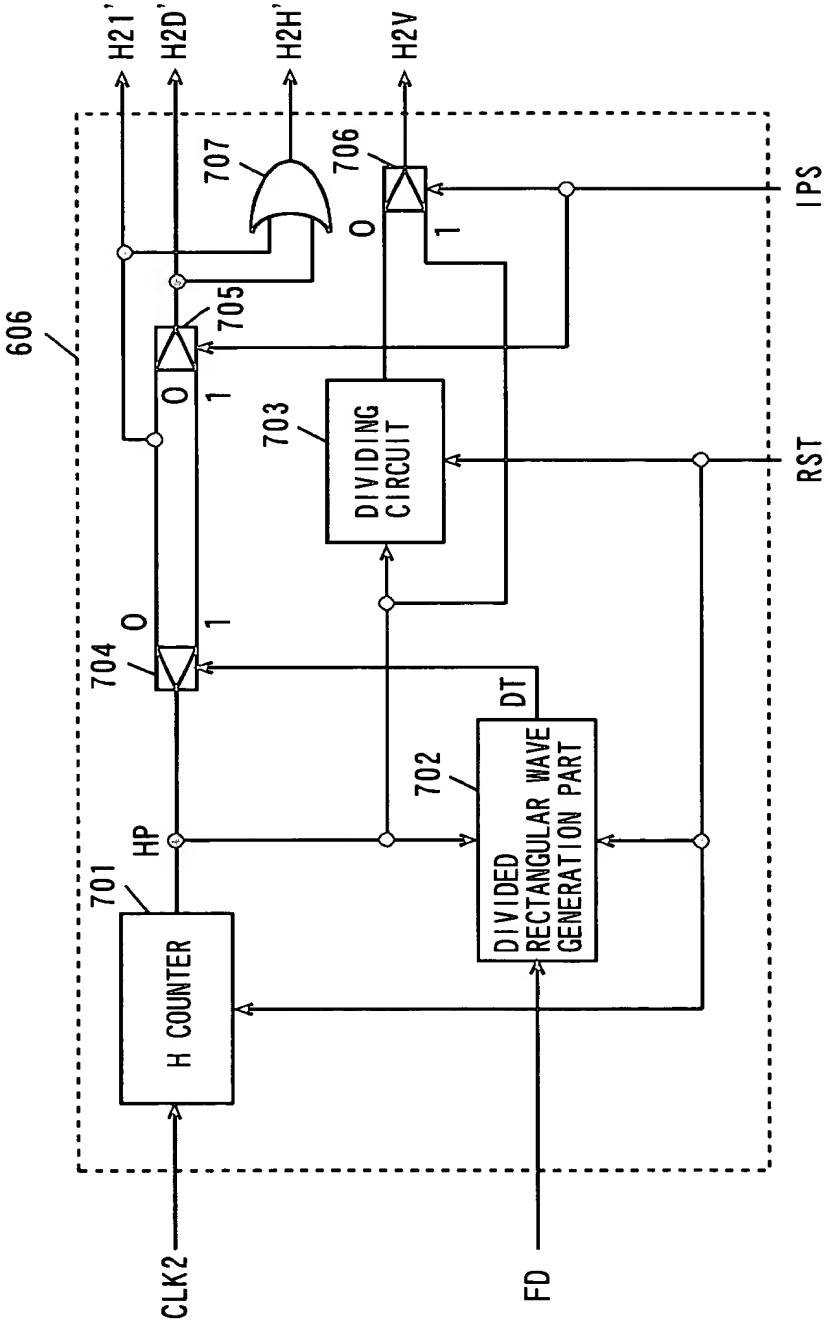

H21'
H2D'
H2H'
H2V
606
707
706
705
703
DIVIDING CIRCUIT
704
702
DIVIDED RECTANGULAR WAVE GENERATION PART
DT
HP
701
H COUNTER
CLK2
FD
IPS
RST
0
1

FIG. 34

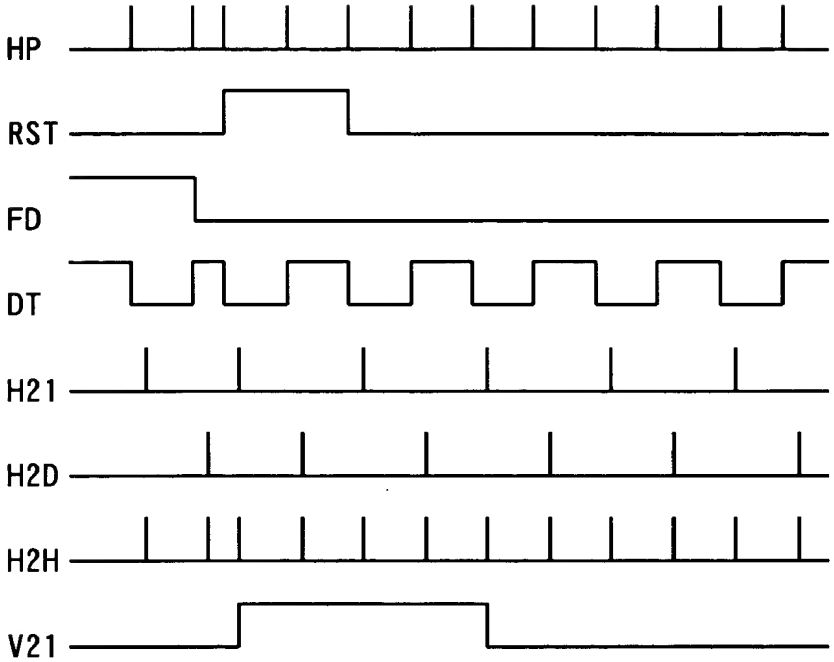


FIG. 35

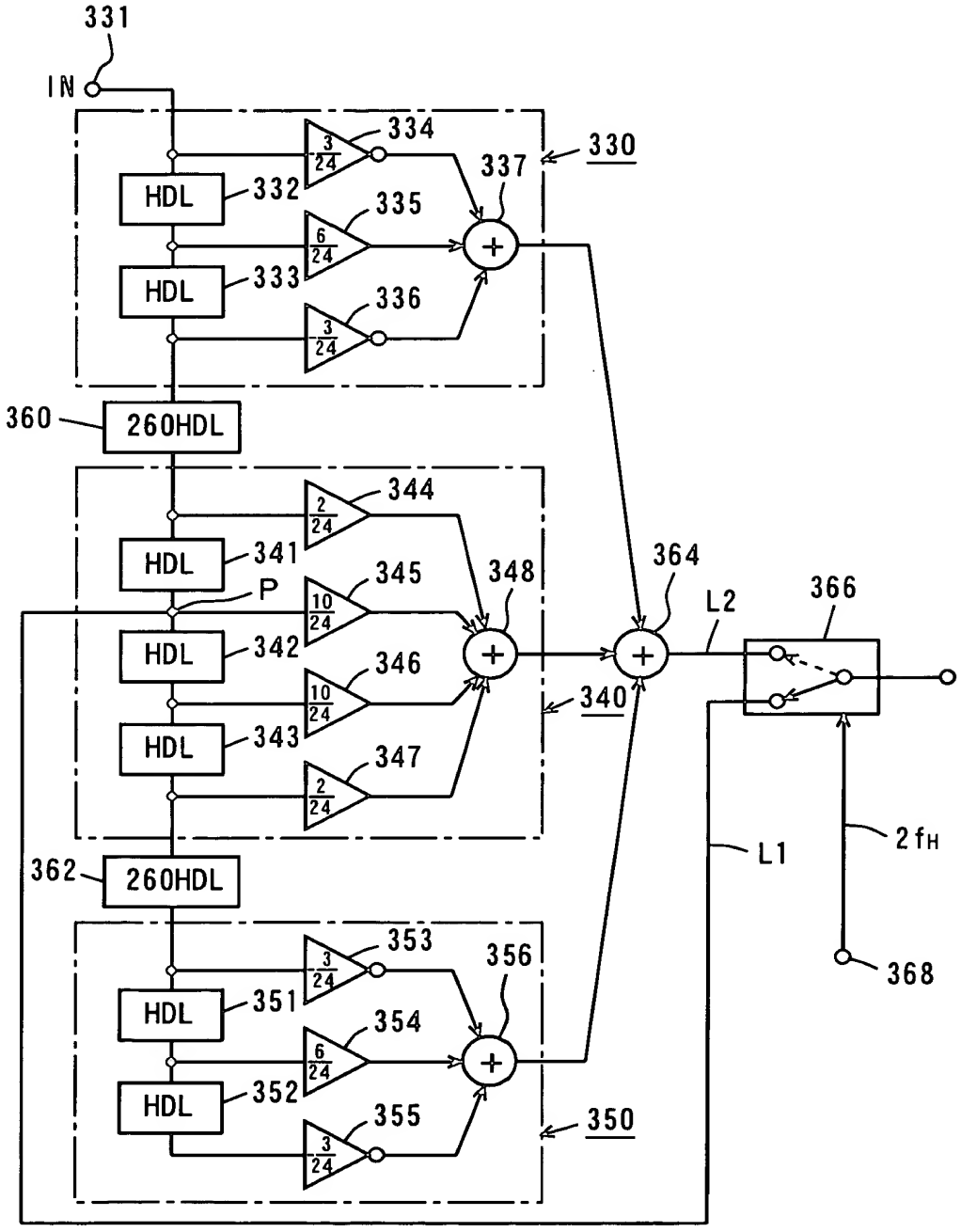

331
IN
330
334
337
335
336
HDL
332
HDL
333
360
260HDL
344
341
345
348
364
366
L2
P
342
346
340
343
347
HDL
HDL
362
260HDL
353
356
351
354
HDL
352
355
350
L1
2fH
368

FIG. 36

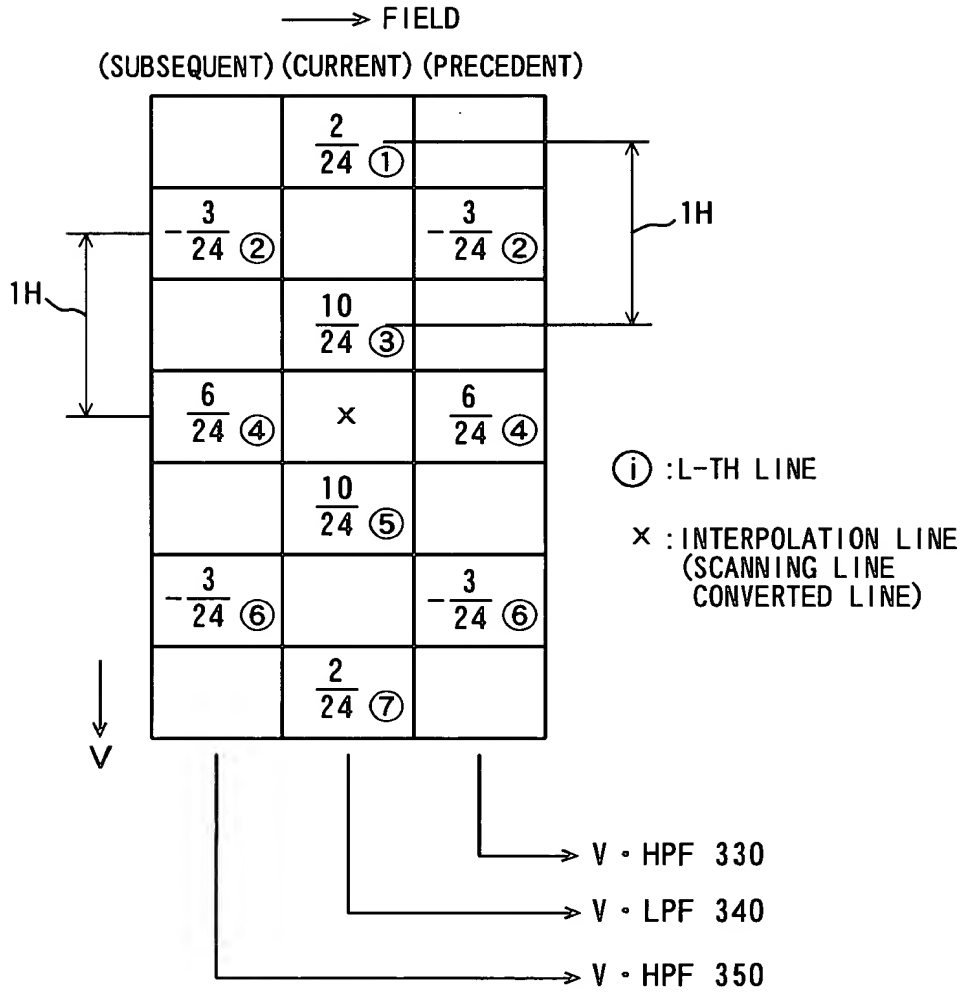
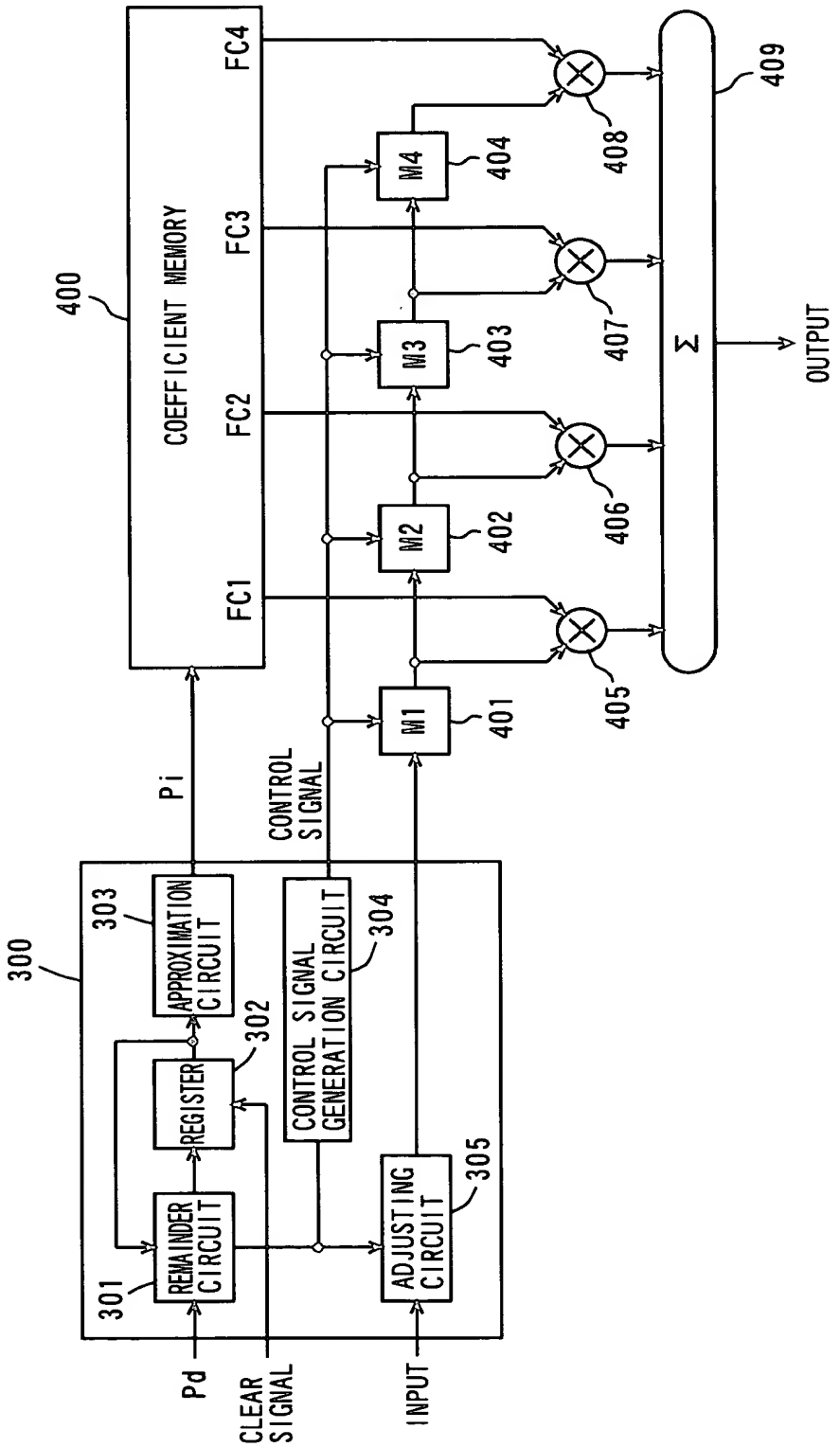

FIELD
(SUBSEQUENT) (CURRENT) (PRECEDENT)
2/24 ①
-3/24 ②
-3/24 ②
10/24 ③
6/24 ④
×
6/24 ④
10/24 ⑤
-3/24 ⑥
-3/24 ⑥
2/24 ⑦
1H
1H
V
ⓘ :L-TH LINE
× :INTERPOLATION LINE (SCANNING LINE CONVERTED LINE)
V・HPF 330
V・LPF 340
V・HPF 350

FIG. 37


300
301
REMAINDER CIRCUIT
REGISTER
302
303
APPROXIMATION CIRCUIT
304
CONTROL SIGNAL GENERATION CIRCUIT
305
ADJUSTING CIRCUIT
Pd
CLEAR SIGNAL
INPUT
Pi
CONTROL SIGNAL
400
COEFFICIENT MEMORY
FC1
FC2
FC3
FC4
M1
M2
M3
M4
401
402
403
404
405
406
407
408
409
Σ
OUTPUT